What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate having an upper surface;

a plurality of adjacent line patterns formed on the upper surface of the semiconductor substrate, each line pattern including a line having a capping layer pattern stacked thereon;

a material layer covering the upper surface of the semiconductor substrate having the line patterns;

a pad contact hole, located between the line patterns within a region of the material layer, which includes a lower opening between the line patterns and an upper opening located above the lower opening;

a barrier layer formed on a side wall defining the upper opening; and

a landing pad substantially filling the lower opening and the upper opening defined by the barrier layer.

2. The semiconductor device according to claim 1, further comprising: line spacers formed on the side walls of the line patterns.

3. The semiconductor device according to claim 1, wherein the line patterns are word line patterns.

4. The semiconductor device according to claim 2, wherein the line spacers are word line spacers.

5. The semiconductor device according to claim 1, wherein the line patterns are bit lines.

6. The semiconductor device according to claim 2, wherein the line spacers are bit line spacers.

7. The semiconductor device according to claim 1, wherein the material layer includes a separation insulating layer and a separation etching stop layer stacked thereon.

8. The semiconductor device according to claim 1, wherein the material layer includes an oxide layer and a nitride layer stacked thereon.

9. The semiconductor device according to claim 1, wherein each respective barrier layer and capping layer pattern is a nitride layer.

10. The semiconductor device according to claim 2, wherein the line spacers are a nitride layer.

11. A method of manufacturing a semiconductor device comprising:

providing a semiconductor substrate;

forming a plurality of adjacent line patterns on the semiconductor substrate;

forming line spacers on the side walls of the line patterns;

forming a material layer on the upper surface of the semiconductor substrate between the adjacent line patterns;

etching a predetermined portion of the material layer to form an upper opening in the material layer between the line patterns;

forming a barrier layer on a side wall defining the upper opening;

etching the material layer below the upper opening defined by the barrier layer to form a lower opening within the material layer exposing the line spacers between the line patterns; and

forming a landing pad by filling the upper opening and the lower opening, respectively.

12. The manufacturing method of claim 11, wherein the formation of the line patterns comprises:

sequentially forming a conductive layer and a capping insulating layer on the semiconductor substrate; and sequentially patterning the capping insulating layer and the conductive layer.

13. The manufacturing method of claim 11, wherein the material layer is formed of a separation insulating layer and a separation etching stop layer stacked thereon.

14. The manufacturing method of claim 13, wherein the separation insulating layer is formed of an oxide layer.

15. The manufacturing method of claim 11, wherein the barrier layer is formed from an insulating layer.

16. The manufacturing method of claim 11, further comprising removing a natural oxide layer and a polymer layer formed in the lower opening, if present, prior to forming the landing pad.

17. The manufacturing method of claim 11, wherein the upper opening is formed so that its bottom surface is no higher than the upper surface of each of the line patterns.

18. A method of manufacturing a DRAM cell array region comprising:

providing a semiconductor substrate;

filling a predetermined region of the semiconductor substrate with a trench isolation layer to form an active region;

forming a plurality of first line patterns on an upper portion of the active region;

forming a plurality of second line patterns, substantially simultaneously with the formation of the first line patterns, on an upper portion of the trench isolation layer adjacent to at least one side of the active region, wherein at least one second line pattern is formed in parallel with the first line pattern and on a side opposite to the first line pattern;

forming line spacers on side walls of the first and second line patterns;

forming a material layer covering the upper surface of the semiconductor substrate;

etching a portion of the material layer to form an upper bit line opening located in a first region between the first line patterns, a first upper storage opening located in a second region between the first and the second line patterns, and a second upper storage opening located in a third region between the first and the second line patterns, respectively;

forming barrier layers on the side walls defining the upper bit line opening, the first upper storage opening, and the second upper storage opening;

etching the material layer below the upper bit line opening, the first upper storage opening, and the second upper storage opening defined by the barrier layers, to form respectively a lower bit line opening, a first lower storage opening, and a second lower storage opening, by penetrating the first region, the second region, and the third region to expose the first and second line patterns; and

forming a bit line landing pad, a first storage landing pad, and a second storage landing pad by filling the lower and upper bit line openings, the first lower and upper storage openings, and the second lower and upper storage openings respectively.

19. The manufacturing method according to claim 18, wherein the upper bit line opening, the first upper storage opening, and the second upper storage opening are formed so that their respective bottom surfaces are no higher than the upper surface of each of the first and second line patterns.

20. The manufacturing method according to claim 18, wherein the material layer includes an oxide layer having a nitride layer stacked thereon.

21. The manufacturing method according to claim 18, wherein each of the first and second line patterns includes a line having a capping layer pattern stacked thereon.

22. The manufacturing method according to claim 18, wherein the barrier layers and the line spacers are a nitride layer.

23. The manufacturing method according to claim 21, wherein the capping layer pattern is a nitride layer.

24. A DRAM cell array region comprising:

a semiconductor substrate;

a trench isolation disposed in a predetermined region of the semiconductor substrate to define an active region;

a plurality of first line patterns on an upper portion of the active region;

a plurality of second line patterns, formed on an upper portion of the trench isolation layer adjacent to at least one side of the active region, wherein at least one second line pattern is formed in parallel with the first line pattern and on a side opposite to the first line pattern;

line spacers formed on side walls of the first and second line patterns;

a material layer covering the upper surface of the semiconductor substrate;

an upper bit line opening located in a first region between the first line patterns, a first upper storage opening located in a second region between the first and the second line

patterns, and a second upper storage opening located in a third region between the first and the second line patterns;

barrier layers formed on the side walls defining the upper bit line opening, the first upper storage opening, and the second upper storage opening;

a lower bit line opening, a first lower storage opening, and a second lower storage opening formed by penetrating the first region, the second region, and the third region to expose the first and second line patterns; and

a bit line landing pad, a first storage landing pad, and a second storage landing pad which fill the lower and upper bit line openings, the first lower and upper storage openings, and the second lower and upper storage openings respectively.

25. The DRAM cell array region according to claim 24, wherein the material layer includes an oxide layer having a nitride layer stacked thereon.

26. The DRAM cell array region according to claim 24, wherein each of the first and second line patterns includes a line having a capping layer pattern stacked thereon.

27. The DRAM cell array region according to claim 24, wherein barrier layers and the line spacers are a nitride layer.

28. The DRAM cell array region according to claim 26, wherein the capping layer pattern is a nitride layer.

29. The DRAM cell array region according to claim 24, wherein the upper bit line opening, the first upper storage opening, and the second upper storage opening are formed so that their respective bottom surfaces are no higher than the upper surface of each of the first and second line patterns.